Remarks/Arguments:

The office action dated July 8, 2007 made the following assertions:

- The drawings are objected for failing to show reference number 38;
- Claims 1-10 and 20 are objected for informalities;
- Claims 1-4, 7, 9-12, and 20 are rejected under 35 USC 102(e) as anticipated by Walton (US 6785341);
- Claims 5-6 and 13-16 are rejected under 35 USC 103(a) as obvious over Walton in view of Catreux (US 2005/0053170);
- Claims 8 and 17 are rejected under 35 USC 103(a) as obvious over Walton in view of Salvi (US 2004/139383);
- Claims 18-19 are rejected under 35 USC 103(a) as obvious over Walton; and
- Claims 21-23 are rejected under 35 USC 103(a) as obvious over Walton in view of Ling (US 6961388).

A replacement drawing sheet is attached as detailed at page 2 of this paper. Claims 1 and 20 are amended to correct typographical errors. All objections are seen to be overcome.

Claim 1 is amended with the subject matter of claim 5, and claim 11 is amended with the subject matter of claims 12-13, and claims 5 and 12-13 are canceled herein. Those dependent claims were rejected over Walton in view of Catreux, but the attached Declarations under Rule 131 disqualify Catreux as prior art against this application. Specifically, Exhibit A referenced by those declarations show conception at least as early as June 16, 2003. The earliest date for Catreux is seen to be July 29, 2003.

The undersigned attests to the following as to diligence. The various docket/reference numbers 17678, NC17678, 873.0134 and 873.0134.U1(US) each refer to the subject matter of this application. Between June 16, 2003 and August 18, 2003, Exhibit A and an invention report based thereon was considered by a patent committee of the Nokia Corporation of Espoo, Finland, and on August 18, 2003 the Nokia Corporation tasked the firm Harrington & Smith LLP to

prepare and file a non-provisional US patent application based on that subject matter, as evidenced by Exhibit B. Exhibit C shows diligence in drafting the application during September 2003 when potential outside disclosure and a proposed filing date were considered. Exhibits D and E show diligence in preparing the application during October 2003, when a first draft of the application was sent for inventor review and returned with inventor comments. Exhibit F shows diligence in November 2003 with another draft of the application and inventor comments exchanged between an inventor and the undersigned. The undersigned attests that exhibits B through F are true copies; acknowledges that statements made above are true or made on information believed to be true; and further acknowledges that any willful false statements are punishable by fine or imprisonment or both under 18 USC 1001.

The application was filed on November 21, 2003 with the inventors' declaration signed on November 20, 2003. Therefore conception is shown prior to the earliest date of Catreux and diligence is shown from then until constructive reduction to practice which occurred no later than November 21, 2003 when the subject application was filed with the US patent office.

Being that Catreux is not prior art against this application, amended claims 1 and 11 are seen to be in condition for allowance. Independent claims 21 and 22 are similarly amended and are also seen to be in condition for allowance.

Added claim 24 is seen to recite subject matter beyond any reasonable interpretation of any reference of record or combination of them. Support for claim 24 is seen most clearly at page 11 lines 1-10 and Figure 3. No new matter is added.

The rejection of the independent claims is seen to be in error. Consider claim 1 as representative of a distinction detailed below; the 'encoding' element is explicitly across time and the 'transmitting' elements may be considered an encoding across space since the transmissions are from different antennas. Reference is made to FIG. 1 and page 7 lines 3-14. Embodiments of this invention interleave, within the turbo encoder 24, a series of N systematic bits (informational bits as opposed to parity bits) and encodes those interleaved N bits to a total of M>N bits. This is

different from channel interleaving 25, which interleaves groups of bits as those groups are output from the turbo encoder. Where the turbo encoder 24 outputs the encoded block of M bits, the channel interleaver interleaves that group of M bits with other groups of encoded bits (which may be the same or different sizes depending on the channel interleaver architecture). Claim 1 refers to the group of size M bits as an encoded packet. The bit-interleaving within the turbo encoder is an encoding across time for the N informational bits as recited in claim 1, which dependent claim 7 recites particularly as bit interleaving over the M bits. By FIG. 1, the individual N bits are interleaved and encoded in the interleaving turbo encoder 24 to a packet of size M, that M-bit encoded packet is interleaved with other packets at the channel interleaver 25 and the channel interleaved encoded packets are mapped to a signal constellation at the mapper 26. That single packet of size M is subdivided into two (or more) separate sub-packets at a demultiplexer 30. By transmitting those separate sub-packets by different transmit antennas 48 and 50 as claim 1 recites, the original encoded packet of size M is encoded across space.

Walton does not encode a plurality of N information bits across time prior to channel interleaving. Walton splits input data into groups at a demultiplexer 208, but separately processes each of those groups in parallel channel data processors 210A, ...210N. Walton does not disclose that the encoder 212 within any of those channel data processors interleaves the bits fed into it. Walton employs channel interleaving, but Walton's channel interleaver 214 is seen to operate substantially as described above: interleaving cohesive groups of bits that are output from the encoder 212 with other cohesive groups of bits from the same encoder 212. Channel interleaving is understood in the art as a form of block interleaving where the groups/blocks being interleaved at the channel interleaver 25 are specific to the channel over which they will be transmitted, whereas block interleaving does not imply a channel-wise restriction to the interleave. Regardless, in Walton these groups of bits are then multiplexed with similar interleaved groups of bits from the other streams S_1, ...S_{NR} and demultiplexed at Walton's demultiplexer 222 for transmission from the different antennas 124A, ...124T. The application as filed distinguishes explicitly over the Walton approach at page 7 lines 3-6:

> Because the present invention inputs the initial packet of N bits into a single turbo encoder 24 (as opposed to splitting the N bits into separate blocks that are input into parallel turbo coders), it enables the initial packet of size N to be interleaved

as a whole at the interleaver within the turbo encoder 24.

Walton splits the bits into parallel streams prior to encoding. If one follows a group of N>1 bits through Walton's FIG. 2 through one of the channel data processors 210A, ...210N, it is not seen that those N bits are encoded across both space and time. If instead one assumes the N systematic bits are split in Walton among the various streams, then the Walton parallel architecture prohibits those N bits across parallel streams from being encoded across time into an encoded packet of M bits that is later divided into first and second transmission packets as claim 1 recites.

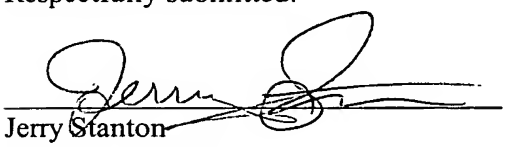
It is seen that Walton gains time and space diversity by splitting the information bits at the demultiplexer 208 among the various streams D_1,... D_{NC}. But Walton does not disclose the granularity of encoding over time or space that claim 1 recites: a plurality of bits are encoded across time; and it is that plurality of bits that are then also encoded across space by transmission from the different first and second transmit antennas. Each of what in Walton might be considered an encoded packet is what is output from the encoder 212, and there is no disclosure that any of the encoders 212 also interleave.

To make more clear that it is the N bits that are encoded over time, added claims 25-28 recite a channel interleaving element, support for which lies at the channel interleaver 25 of FIG. 2 and at page 7 lines 9-10. No new matter is added. The only interleaving disclosed in a Walton transmitter is the channel interleaver 214, which does not encode on a bit level across time but rather on a block level, where the blocks are designated by channel. Walton discloses no encoding across time prior to channel interleaving as claims 25-28 now recite. Claims 25-28 are therefore seen to be novel and non-obvious over Walton alone or in combination with any other cited art. The above further demonstrates that Walton does not anticipate claims 1 or 11 and its correlation to claims 21 and 22 is less than the office action asserts.

Regardless, the amendments made herein and the attached declaration under Rule 131 and the related statements above as to diligence put each and every claim in condition for allowance

given the findings of the office action itself. The Applicants thank the Examiner for the search and detailed remarks, and now requests him to withdraw the rejections and pass claims 1-4, 6-11 and 14-28 to issue. The undersigned representative welcomes the opportunity to resolve any matters that may remain, formal or otherwise, via teleconference at the Examiner's discretion.

Respectfully submitted:



December 5, 2007
Date

Jerry Stanton
Reg. No.: 46,008

Customer No.: 29683
HARRINGTON & SMITH, PC
4 Research Drive
Shelton, CT 06484-6212
Phone: (203) 925-9400, ext 12
Facsimile: (203) 944-0245
Email: gstanton@hspatent.com

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

12/5/2007
Date

Claire F. Mann
Name of Person Making Deposit